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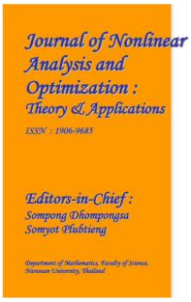

DESIGN LOW POWER PERFORMANCE PROPOSED FULL-ADDER ARCHITECTURE

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ABSTRACT:

Full adder is an essential component for the design and development of all types of processor. This is widely used to implement Full Adder (FA) circuits. Performance of FA in terms of delay, power, and capability is largely dependent on the performance of circuit. Researchers are increasingly interested in spintronic technology-based electronic circuits due to their low power consumption, non-volatility, and compatibility with CMOS technology. However, these circuits usually rely on the pre charge sense amplifier (PCSA), to read the state of the magnetic tunnel junctions (MTJ). PCSAs have a significant disadvantage due to their high sensitivity to input scheduling, causing invalid output if inputs aren't applied correctly within the specified time, then causes a significant issue in ripple carry adders due to their propagation. Therefore, to overcome the above issue proposed a post-processing unit, which makes the spintronic adders invulnerable to inputs scheduling. In this adder we are making 64 Bit cascadable adder. Xilinx is the software used in this project.

KEYWORDS: Low-Power, Full-Adder, Ripple Carry Adder, Spintronic, Magnetic Tunnel Junction (MJT), Cascadable Adders.

INTRODUCTION

In the past decades, the major challenge for the VLSI designer was area, performance, cost and power consumption. In recent years,the trend for CMOS technology has improved and need to integrate more functions in a given silicon area. According to Moore's law, number of transistor in a chip doubles every two year at the same time the cost of the computer is halved. In detail, the speed and capability of computer increases for every two year and cost will reduced. As increase in no. oftransistor in a chip, power will be increased and processing time of each transistor also increases. Thus, there will be loss in performance, to compensate for the performance loss use of either parallel or pipelined implementations [2]. A parallel implementation just doubles hardware thus pipelining is for low power solutions. Many full adder circuits were designed using various logic styles; each of them has its own merits and demerits. A full adder is a basic circuit that does all computations from counting to multiplication to filtering. A fast and accurate operation of a digital system is greatly influenced by the performance ofthe resident adders.These in turn, form the core of any system and thereby influence the overall performance of the entire system.

LITERATURE SURVEY

Bio-inspired nonvolatile and low-cost spin-based 2-bit per cell memory by A. Amirany, M. H. Moaiyeri, and K. Jafari.

To deal with the daily increase of the power consumption and area overhead of the memory cells, in this paper a bio-inspired nonvolatile spin-based 2-bit per cell memory circuit is proposed. Multi-level memory (MLM) cells are capable of storing more than a single bit of information in a single memory cell. MLM architecture offers lower cost per unit of storage due to the higher data density, lower area per stored bit and most importantly lower power consumption. Thanks to the nonvolatile feature of the magnetic tunnel junction (MTJ), the proposed MLM memory can be powered off during the idle cycles in order to reduce the static power consumption. The simulation results even at the corners of the fabrication process indicate that the proposed MLM memory occupies up to 33.33% lower area and consumes 82.95% lower power per bit of the stored data in comparison to the previous nonvolatile spintronic memories.

Low-power and fast full adder by exploring new XOR and XNOR gates by H. Naseri and S. Timarch.

In this project, novel circuits for FULL ADDER are proposed using new XOR or XNOR gates. The conventional design of XOR or XNOR gates shows that the not gate in the schematic has drawbacks. So by investigating advanced XOR or XNOR gates we proposed the schematic design. The proposed schematics are optimized in terms of speed, delay, power and power delay product. We developed six novel hybrid full adder schematics based on exploring new XOR or XNOR gates. Each designed schematics have their specifications of energy consumption, delay, power delay product. To simulate the performance of the proposed designs, we use mentor graphics, tanner tool. The simulation yields a 45-nm CMOS innovation model that focuses on the proposed plans having best speed and power other than the plan of any full adder. The proposed Full Adders has 2-28% increment in consumption of energy and power delay product compared to other design schematics. The proposed hybrid full adders are investigated with voltage 1.8V, speed ,size of transistors, area, power consumption and delay.

A novel high-speed lowpower binary signed-digit adder by S. Timarchi, P. Ghayour, and Shahbahrami.

Addition is one of the most important arithmetic operations in digital computation. Optimization of adders' speed, power, and area is a challenging task. To this end, redundant number system has been proposed in the literatures. In this paper, we propose a new suvredundant binary signed-digit adder that not only utilizes specific encoding for the input operands, but also uses a new efficient adder structure. Using this technique we can generate low power signed digit adders that perform fast additions. The comparisons show delay, power and area reduction both on FPGA and Synopsys Design Vision tool.

Low power magnetic full-adder based on spin transfer torque by E. Deng, Y. Zhang, J.-Klein, D. Ravelsona, C. Chappert, and W. Zhao.

Power issues have become a major problem of CMOS logic circuits as technology node shrinks below 90 nm. In order to overcome this limitation, emerging logic-in-memory architecture based on nonvolatile memories (NVMs) are being investigated. Spin transfer torque (STT) magnetic random access memory (MRAM) is considered one of the most promising NVMs thanks to its high speed, low power, good endurance, and 3-D back-end integration. This paper presents a novel magnetic full-adder (MFA) design based on perpendicular magnetic anisotropy (PMA) STT-MRAM. It provides advantageous power efficiency and die area compared with conventional CMOS-only full adder (FA). Transient

simulations have been performed to validate this design by using an industrial CMOS 40 nm design kit and an accurate STT-MRAM compact model including physical models and experimental measurements.

EXISITING SYSTEM

One of the disadvantages of PCSAbased circuits is their sensitivity to the input's scheduling. If the inputs are not applied to the circuit simultaneously and at the zero level of the clock signal (pre-charge phase), the produced result at the output may not be valid. On the other hand, carry is generated by a full-adder in the Ripple Carry Adder structure, and then transferred to the next fulladder. Considering this issue, in the PCSA-based spintronic adders, invalid output maybe generated. The circuit shown in Fig. 2 is proposed to address this problem. In this circuit, the main input operands (A and B) are initially processed. Then, the intermediate signals (S and C) are generated based on the inputs. By utilizing these signals and the carry of the previous level (Ci), the sum and the output carry (Cout) are generated and transferred to the next level. Since the carry only enters the post-processing unit in the proposed circuit, the propagation delay of the carry does not affect the PCSA circuit performance. The proposed circuit also uses 8 reconfigurable MTJ cells and 2 fixed MTJ, which has 4 reconfigurable MTJ cells less than the best available circuit is presented . Moreover, given that the majority of the power is consumed to configure the MTJs, the proposed circuit consumes less power than the previous circuits . Table I shows the truth table of the various part of the proposed circuit. According to Table I, the logical functions of the Cout and Sum are given by the equations (2) and (3):

$$Cout = Ci \cdot S + C \qquad \text{…….(2)}$$

$$Sum = Ci \cdot S' + Ci \text{ '}\cdot C' \cdot S \qquad \text{…….(3)}$$

where C and S are given by equations (4) and (5).

$$C = A \cdot B \qquad \text{……. (4)}$$

$$S = A \oplus B \qquad \text{……. (5)}$$

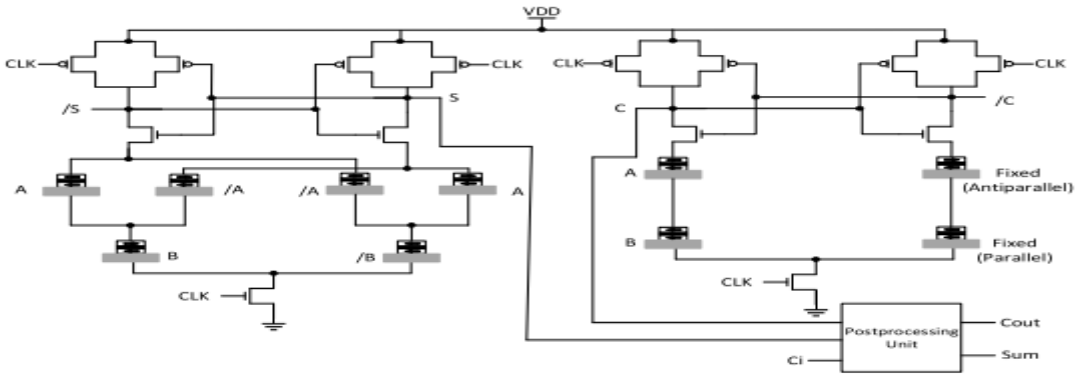


Fig. cascadable spintronic Full-Adder

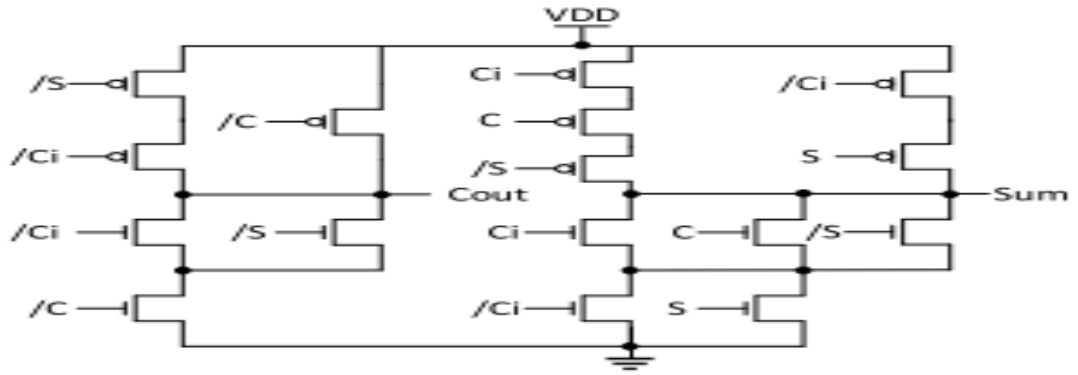


Fig.Post Processing block of cascadable spintronic Full-Adder

The proposed circuit was simulated by the HSpice software using the 32nm CMOS transistors model and the MTJ model is presented. The specifications of the MTJ are provided in Table II. The supply voltage is considered to be 1V in all simulations. The existing circuits had been simulated with different technologies, i.e., the MFAs is presented had been simulated with CMOS 28nm, CMOS 40nm, and CMOS 32nm, respectively. However, to have a fair comparison, all existing circuits were optimized to have the best latency. The Post-processing block of the proposed full-adder. identical input patterns under the same conditions using 32nm CMOS technology.

To design a low-power performance Full Adder architecture, we can focus on reducing power consumption by optimizing various aspects of the circuit. Here's a proposed approach:

- Use of Low-Power Logic Gates*: Implement the Full Adder using low-power logic gates such as CMOS (Complementary Metal-Oxide-Semiconductor) gates. This can include using techniques like transmission gate logic or pass transistor logic, which can reduce power consumption compared to traditional CMOS gates.

- Clock Gating*: Incorporate clock gating techniques to disable the clock signal to unused parts of the circuit when they are not needed. This helps in reducing dynamic power consumption.
- Voltage Scaling*: Operate the circuit at lower supply voltages to reduce power consumption. However, this needs to be balanced with maintaining circuit performance and reliability.
- Use of Sleep Transistors*: Integrate sleep transistors into the circuit to effectively cut off power supply to inactive parts of the circuit, further reducing leakage power.
- Power Gating*: Implement power gating techniques to completely isolate parts of the circuit when they are not in use, thereby reducing both leakage and dynamic power consumption.
- Transistor Sizing*: Optimize transistor sizing to minimize power consumption while meeting performance requirements. This involves carefully selecting transistor sizes to balance speed and power.
- Circuit Partitioning*: Partition the Full Adder circuit into smaller blocks and optimize each block individually for power efficiency. This allows for better optimization and reduces overall power consumption.
- Advanced Power Management Techniques*: Explore advanced power management techniques such as dynamic voltage and frequency scaling (DVFS) to dynamically adjust the operating voltage and frequency based on workload requirements.

By incorporating these techniques, you can design a low-power performance Full Adder architecture that meets the desired power consumption requirements while maintaining adequate performance.

SIMULATION RESULTS & SYNTHESIS REPORT

EXISTING METHOD RTL SCHEMATIC:

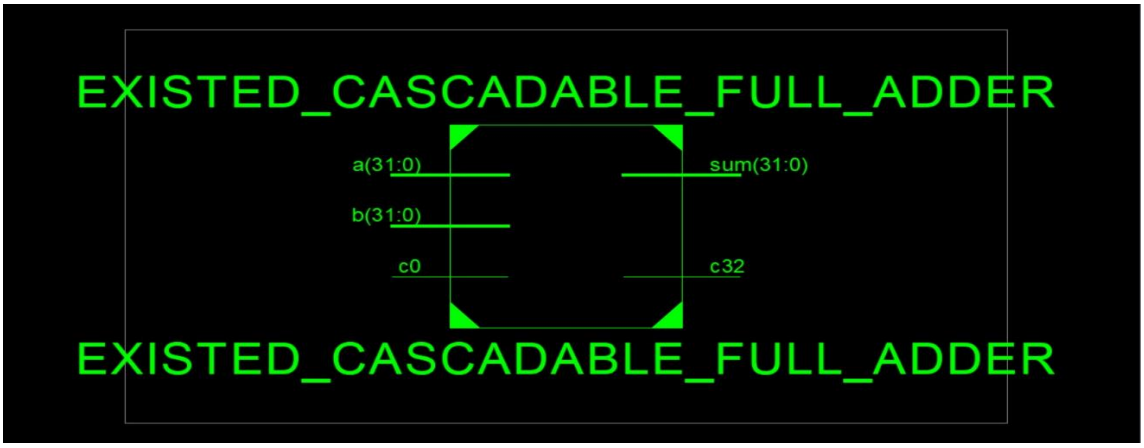


Fig. Existing Method cascadable Full-Adder

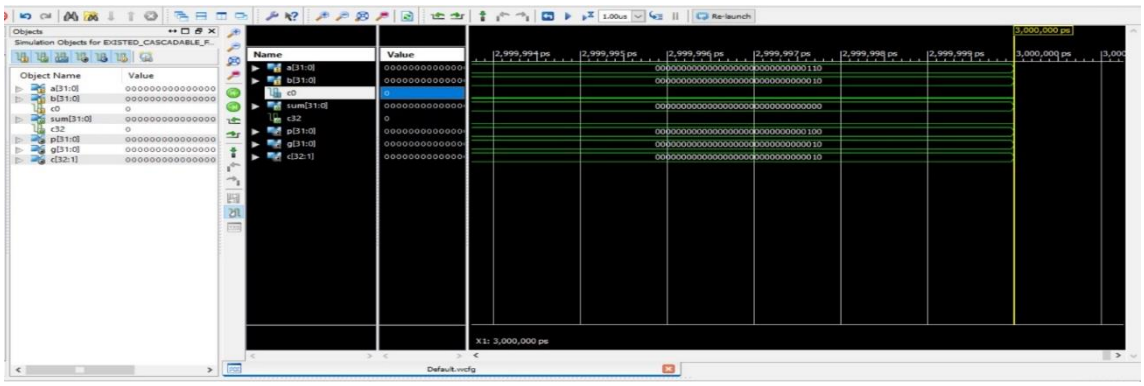


Fig. Simulation Results of Existing Method cascadable Full-Adder

Power:

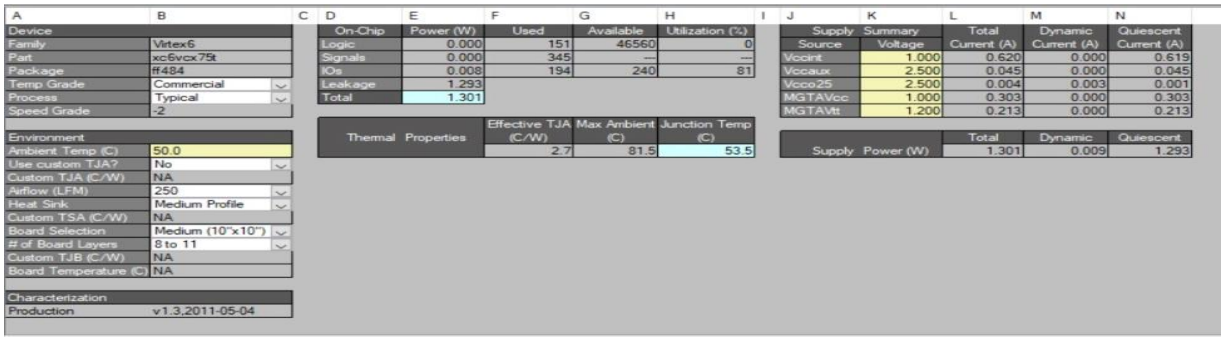
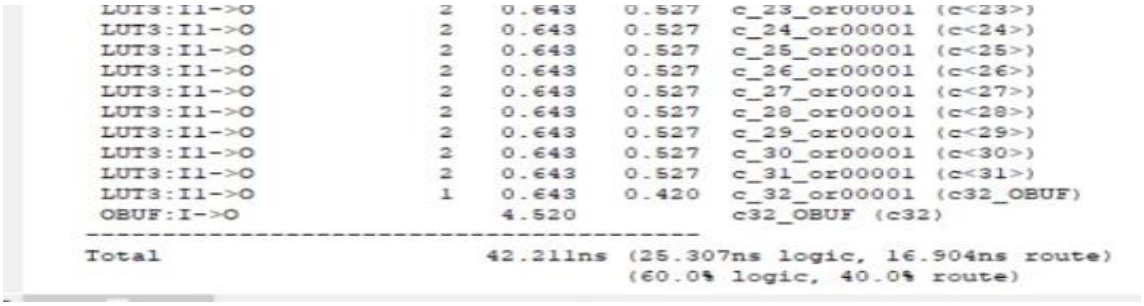


Fig. Power of Existing Method cascadable Full-Adder

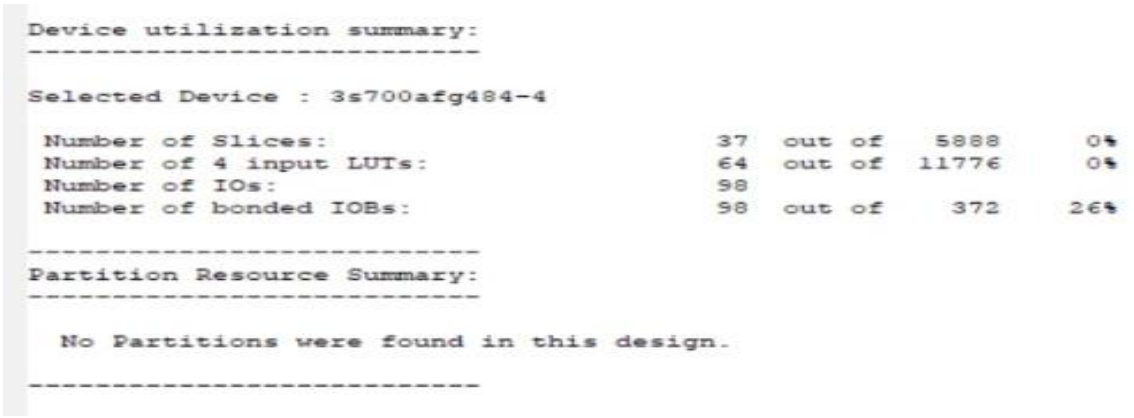
Delay:



```
LUT3:I1->O            2    0.643    0.527  c_23_or00001 (c<23>)
LUT3:I1->O            2    0.643    0.527  c_24_or00001 (c<24>)
LUT3:I1->O            2    0.643    0.527  c_25_or00001 (c<25>)
LUT3:I1->O            2    0.643    0.527  c_26_or00001 (c<26>)
LUT3:I1->O            2    0.643    0.527  c_27_or00001 (c<27>)
LUT3:I1->O            2    0.643    0.527  c_28_or00001 (c<28>)
LUT3:I1->O            2    0.643    0.527  c_29_or00001 (c<29>)
LUT3:I1->O            2    0.643    0.527  c_30_or00001 (c<30>)
LUT3:I1->O            2    0.643    0.527  c_31_or00001 (c<31>)
LUT3:I1->O            1    0.643    0.420  c_32_or00001 (c32_OBUF)
OBUF:I->O                  4.520            c32_OBUF (c32)
----------------------------------------
Total                     42.211ns (25.307ns logic, 16.904ns route)
                                   (60.0% logic, 40.0% route)
```

Fig. Delay of Existing method cascadable Full-Adder

Utilization:



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Device utilization summary:
---------------------------

Selected Device : 3s700afg484-4

 Number of Slices:                       37  out of   5888     0%
 Number of 4 input LUTs:                 64  out of  11776     0%
 Number of IOs:                          98
 Number of bonded IOBs:                  98  out of    372    26%

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Partition Resource Summary:
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  No Partitions were found in this design.

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```

Fig. Utilization of Existing method cascadable Full-Adder

PROPOSED METHOD RTL SCHEMATIC:

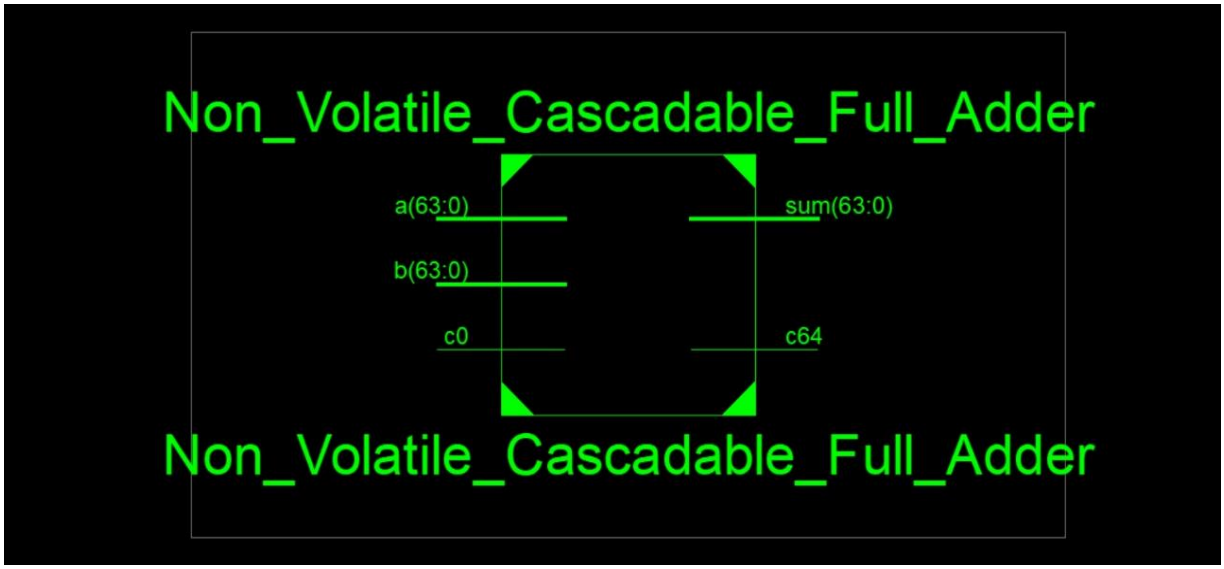

Fig. Proposed Method cascadable Full-Adder

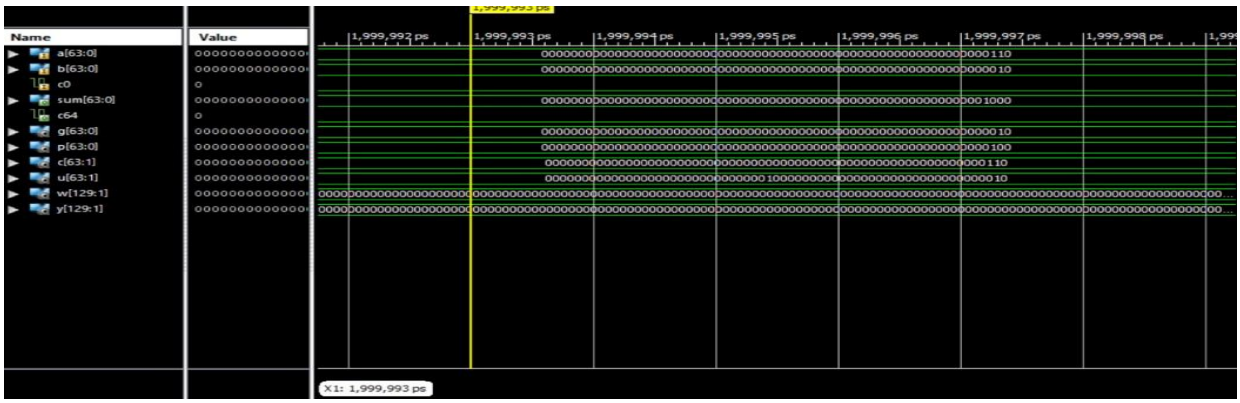

Fig. Simulation Results of Proposed Method cascadable Full-Adder

Power:

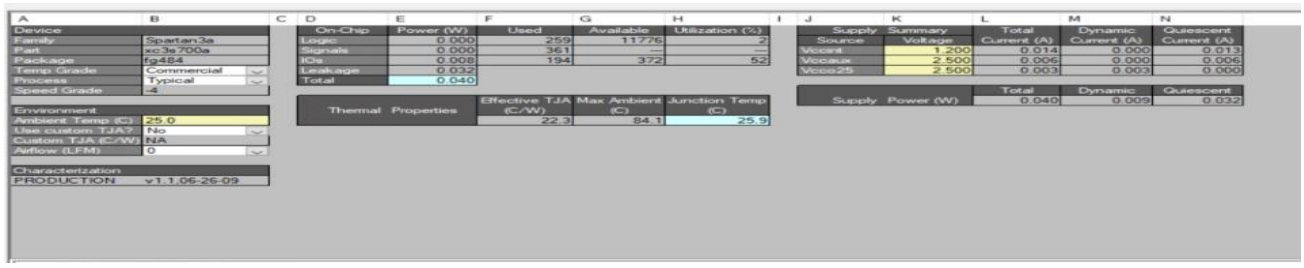

Fig. Power of Proposed Method cascadable Full-Adder

Delay:

```
LUT3:I2->O            1    0.648    0.452  u<24>11 (u<24>11)
LUT4:I2->O            4    0.648    0.619  u<24>30 (u<24>)
LUT4:I2->O            1    0.648    0.423  gc32/G10 (gc32/G10)
LUT4:I3->O            1    0.648    0.563  gc32/G87_SW0 (N175)
LUT3:I0->O            1    0.648    0.452  gc32/G129_SW0_SW0 (N177)
LUT4:I2->O            1    0.648    0.452  gc32/G129_SW0 (N167)
LUT3:I2->O            2    0.648    0.527  gc32/G129 (u<32>)
LUT3:I1->O            1    0.643    0.420  c641 (c64_OBUF)
OBUF:I->O                  4.520          c64_OBUF (c64)
----------------------------------------
Total                     32.490ns (20.268ns logic, 12.222ns route)
                                   (62.4% logic, 37.6% route)
```

Fig. Delay of Proposed Method cascadable Full-Adder

Utilization:

```
Device utilization summary:
---------------------------

Selected Device : 3s700afg484-4

 Number of Slices:                      145  out of   5888      2%
 Number of 4 input LUTs:                259  out of  11776      2%
 Number of IOs:                         194
 Number of bonded IOBs:                 194  out of    372     52%

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Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

Fig. Utilization of Proposed Method cascadable Full-Adder

CONCLUSION

Full adder is an essential component for the design and development of all types of processor. This is widely used to implement Full Adder (FA) circuits. Performance of FA in terms of delay, power, and capability is largely dependent on the performance of circuit. Researchers are increasingly interested in spintronic technology-based electronic circuits due to their low power consumption, non-volatility, and compatibility with CMOS technology. Spintronic circuits have drawn the attention of many researchers in recent years. Full-adders are one of these circuits. The circuit proposed in this brief uses a post-processing unit to generate the final output. Hence, this 64-bit is compatible for the high level applications. Therefore, to overcome the above issue proposed a post-processing unit, which makes the spintronic adders invulnerable to inputs scheduling. In this adder we are making 64 Bit cascadable adder.

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